CLAIMS

1. A method of fabricating a semiconductor device comprising:

providing a semiconductor heterostructure, said heterostructure comprising a relaxed $Si_{1-x}Ge_x$ layer on a substrate, a strained channel layer on said relaxed $Si_{1-x}Ge_x$ layer, and a $Si_{1-y}Ge_y$ layer;

removing said $Si_{1-y}Ge_y$ layer; and

providing a dielectric layer.

2. The method of claim 1, wherein said $Si_{1-y}Ge_y$ layer is removed by a selective technique.

3. The method of claim 2, wherein said selective technique is wet oxidation below 750°C.

4. The method of claim 2, wherein said selective technique is a wet or dry chemical etch.

5. The method of claim 1, wherein said dielectric layer comprises a gate dielectric of a MISFET.

6. The method of claim 5, wherein the gate dielectric comprises an oxide.

7. The method of claim 5, wherein the gate dielectric is deposited.

8. The method of claim 5, wherein the MISFET comprises a surface channel device.

9. The method of claim 5, wherein the MISFET comprises a buried channel device.

10. The method of claim 1, wherein the strained channel layer comprises Si.

11. The method of claim 1, wherein x is approximately equal to y.

12. The method of claim 11 further comprising a sacrificial Si layer on said sacrificial $Si_{1-y}Ge_y$ layer.

13. The method of claim 1, wherein $y > x$.

14. The method of claim 13 further comprising a sacrificial Si layer on said sacrificial $Si_{1-y}Ge_y$ layer.

15. The method of claim 14, wherein the thickness of the sacrificial Si layer is greater than the critical thickness.

16. The method of claim 1, wherein the substrate comprises Si.

17. The method of claim 1, wherein the substrate comprises Si with a layer of SiO_2.

18. The method of claim 1, wherein the substrate comprises a SiGe graded buffer layer on Si.

19. The method of claim 1, wherein the semiconductor device comprises a MISFET.

20. A method of fabricating a semiconductor device comprising:

providing a semiconductor heterostructure, said heterostructure comprising a relaxed

$Si_{1-x}Ge_x$ layer on a substrate, a strained channel layer on said relaxed $Si_{1-x}Ge_x$ layer, and a $Si_{1-y}Ge_y$ layer;

removing said $Si_{1-y}Ge_y$ layer to expose said strained channel layer;

removing a portion of said strained channel layer to eliminate any residual Ge; and

providing a dielectric layer.

21. A method of fabricating a semiconductor device comprising:

providing a semiconductor heterostructure, said heterostructure comprising a relaxed $Si_{1-x}Ge_x$ layer on a substrate, a strained channel layer on said relaxed $Si_{1-x}Ge_x$ layer, a $Si_{1-y}Ge_y$ spacer layer, and a $Si_{1-w}Ge_w$ layer;

removing said $Si_{1-w}Ge_w$ layer; and

providing a dielectric layer.

22. The method of claim 21, wherein said dielectric layer comprises the gate dielectric of a MISFET.

23. The method of claim 22, wherein the gate dielectric comprises an oxide.

24. The method of claim 22, wherein the gate dielectric is deposited.

25. The method of claim 22, wherein the MISFET comprises a buried channel device.

26. The method of claim 21, wherein the strained channel comprises Si.

27. The method of claim 21, wherein w is approximately equal to y.

28. The method of claim 27 further comprising a sacrificial Si layer on said sacrificial $Si_{1-w}Ge_w$ layer.

29. The method of claim 21, wherein $w > y$.

30. The method of claim 29 further comprising a sacrificial Si layer on said sacrificial $Si_{1-w}Ge_w$ layer.

31. The method of claim 30, wherein the thickness of the sacrificial Si layer is greater than the critical thickness.

32. The method of claim 21, wherein the substrate comprises Si.

33. The method of claim 21, wherein the substrate comprises Si with a layer of SiO_2.

34. The method of claim 21, wherein the substrate comprises a SiGe graded buffer layer on Si.

35. The method of claim 21, wherein the semiconductor device comprises a MISFET.

36. A method of fabricating a semiconductor device comprising:

providing a semiconductor heterostructure, said heterostructure comprising a relaxed $Si_{1-x}Ge_x$ layer on a substrate, a strained channel layer on said relaxed $Si_{1-x}Ge_x$ layer, a $Si_{1-y}Ge_y$ spacer layer, a Si layer, and a $Si_{1-w}Ge_w$ layer;

removing said $Si_{1-w}Ge_w$ layer to expose said Si layer; and

providing a dielectric layer.

37. A method of fabricating a semiconductor device comprising:

providing a semiconductor heterostructure, said heterostructure comprising a relaxed $Si_{1-x}Ge_x$ layer on a substrate, a strained channel layer on said relaxed $Si_{1-x}Ge_x$ layer, a $Si_{1-y}Ge_y$ spacer layer, a Si layer, and a $Si_{1-w}Ge_w$ layer;

removing said $Si_{1-w}Ge_w$ layer to expose said Si layer; and

oxidizing said Si layer.

38. The method of claim 37, wherein the semiconductor device comprises a MOSFET.

39. The method of claim 37, wherein the semiconductor device comprises a buried channel MOSFET.